4/4 B.Tech. SEVENTH SEMESTER
ELECTIVE – II

EM7T3A DSP PROCESSORS AND ARCHITECTURE Credits: 3

Lecture: 3 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course Objectives:

The purpose of this course is to introduce the concepts of DSP Processor and its architecures.To program DSP Processor for various applications.

Learning Outcomes:
At the end of this course, the students will be able to understand the DSP ProcessorTMS320C5X Understand the implementation of basic DSP algorithms using DSP Processors

UNIT-I
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementations, A/D Conversion Errors, DSP Computational Errors, D/A Conversion Errors.

UNIT-II
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

UNIT-III
EXECUTION CONTROL AND PIPELINING: Hardware Looping, Interrupts, Stacks, Relative Branch Support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects,Interrupt Effects, Pipeline Programming Models.

UNIT-IV
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital Signal-Processing Devices, Data Addressing Modes of TMS320C54XX DSPs, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-V
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT- VI

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and Scaling, Bit-Reversed Index Generation, An 8-Point FFT Implementation on the TMS320C54XX, Computation of the Signal Spectrum.VR10 Regulations

UNIT- VII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSPDEVICESI: Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts And I/O, Direct Memory Access (DMA).

UNIT- VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES -II:A Multi channel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit, CODEC Programming, A CODEC-DSP Interface Example.

Text Book:

1.Avatar Singh and S.Srinivasan,"DSP Processors and Architectures", 2004,Thomson Publications.(Units-I,III& IV)

2. Lapsley et al, "DSP Processor Fundamentals, Architectures & Features" 2000, S. Chand & Co (Unit-II)

Reference Books:

1. B. Venkataramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications" , 2002, TMH.

2. Jonatham Stein, "Digital Signal Processing", 2005, John Wiley.